IN THE CLAIMS

CLAIM 1 (Currently amended) A computer motherboard architecture comprising:

a ~~A~~ computer motherboard possessing typical components including a CPU, a data bus, a power interface, and an audio input data pathway, said audio input data pathway connecting the audio input of the motherboard to the CPU;

a ~~A~~ DSP chip in the audio input data path;

a ~~A PCI-to-DSP~~ bridge interfacing between said DSP chip and the bus on the computer motherboard;

a ~~A~~ memory in electrical connection to said DSP chip;

a ~~A~~ command and control speech engine residing in said memory of said DSP chip; wherein said DSP is enabled to operate in either command and control mode or continuous speech mode and said DSP serves as the preprocessor of all speech input prior to execution of instructions by the CPU to process the speech input.

CLAIM 2 (Cancelled)

CLAIM 3 (Original) A computer motherboard architecture according to claim 1 wherein said DSP is operable to be dynamically set by a user in either a continuous speech mode or a command and control mode.

CLAIM 4 (Currently amended) A computer architecture according to claim 1 wherein said audio input data pathway comprises a microphone input, means for digitizing an

audio input data pathway, and a DSP chip, ~~and a PCI to DSP~~ bridge chip communicating with said bus.

CLAIM 5 (Original) A computer motherboard according to claim 1 wherein said DSP chip is operable to convert said audio input into phonemes.

CLAIM 6 (Original) A computer architecture according to claim 1 wherein said speech engine includes a vocabulary of speech terms which are associated with specific instructions or contextual environments.

CLAIM 7 (Currently amended) A computer architecture according to claim 6 wherein said vocabulary of speech terms resides in said memory in electrical connection to ~~of~~ said DSP chip.

CLAIM 8 (Original) A computer architecture according to claim 6 wherein said vocabulary of speech terms is able to be defined by a user, either in a static or active mode.

CLAIM 9 (Currently amended) A computer architecture according to claim 6 ~~1~~ wherein said vocabulary of speech terms is refreshed by the CPU based upon the context of an application running on a host processor.

CLAIM 10 (Original) A computer architecture according to claim 1 wherein said DSP chip is operable to perform preprocessing for a software-based speech engine residing elsewhere on a computer.

CLAIM 11 (Original) A computer architecture according to claim 1 wherein said DSP chip is operable to perform menu selection such as mobile phone audio functions comprising voice activated dialing, voice control, noise cancellation, and speech to signal conversion.

CLAIM 12 (Original) A computer architecture according to claim 1 wherein said DSP chip is operable to perform noise cancellation functions.

CLAIM 13 (Original) A computer architecture according to claim 1 wherein said DSP chip is operable to function in a command and control speech mode.

CLAIM 14 (Original) A computer architecture according to claim 1 wherein said DSP chip is operable to function in a continuous speech mode.

CLAIM 15 (Original) A computer architecture according to claim 1 wherein said DSP chip is operable to function in a mobile phone mode.

CLAIM 16 (Original) A computer architecture according to claim 1 wherein said DSP is operable to function in a language translation mode.

CLAIM 17 (Original) A computer architecture according to claim 1 wherein said computer motherboard is a user-supported computer motherboard.

CLAIM 18 (Original) A computer architecture according to claim 17 wherein said user-supported computer is a voice activated user-supported computer.

CLAIM 19 (Original) A computer architecture according to claim 1 wherein said computer motherboard is a portable computer motherboard.

CLAIM 20 (Original) A computer architecture according to claim 1 wherein said computer motherboard is a personal digital assistant motherboard.

CLAIM 21 (Original) A computer architecture according to claim 1 wherein said computer motherboard is a desktop computer motherboard.

CLAIM 22 (Original) A computer architecture according to claim 1 wherein said computer motherboard is a hand held computer motherboard.

CLAIM 23 (Original) A computer architecture according to claim 1 wherein said computer motherboard is a video gaming system computer motherboard.

CLAIM 24 (Original) A computer architecture according to claim 1 wherein said computer motherboard is a computing and communications device computer motherboard.

CLAIM 25 (Original) A computer system of claim 1 wherein said computer motherboard is a component of a member selected from the group consisting of user supported computers, laptop computer, desktop computers, portable computers and mixtures thereof.

CLAIM 26 (Original) A computer system according to claim 1 wherein said computer motherboard is a component of a member selected from the group consisting of cell telephones, wireless telephones, portable computers, communication means both hard wired and wireless and mixtures thereof.

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CLAIM 27 (Currently amended) A method of processing speech in a computer, the method comprising:

designating ~~Designating~~ a command and control processing mode;

designating ~~Designating~~ a continuous processing mode;

placing ~~Placing~~ a DSP chip on a motherboard in the audio input data pathway;

placing ~~Placing~~ a ~~DSP-to-PCI~~ bridge chip ~~or equivalent circuitry~~ in series after the DSP chip for communication with said computer's ~~PCI~~ bus;

receiving ~~Receiving~~ a speech input through said audio input data pathway;

if ~~If~~ in said command and control processing mode, said DSP chip converting said speech input to phonemes and matching said phonemes with commands stored in said DSP resident memory to create a CPU instruction;

if ~~If~~ in said continuous mode, said DSP chip converting said speech input into phonemes;

passing ~~Passing~~ off said instruction or said phonemes to a CPU by way of said ~~DSP-to-PCI~~ bridge chip ~~or equivalent path~~ on said motherboard; wherein said DSP serves as the preprocessor of all speech input prior to execution of instructions by the CPU to process the speech input.

CLAIM 28 (Cancelled)

CLAIM 29 (New) A computer architecture according to claim 1 wherein said DSP is operable to accommodate full interpreting and processing of said speech without said CPU being utilized.

CLAIM 30 (New) A computer architecture according to claim 1 wherein said DSP is enabled to substantially reduce power consumption from a like system absent said DSP.

Status of Claims

Claims 1, 3-27 are pending in the instant application having amended claims 1, 4, 7, 9, and 27 to better define the invention.

Claim Objections

Claims 7 and 9 stand objected to because of informalities from lack of antecedent basis for the phrase "a memory in electrical connection to said DSP chip" and "said vocabulary", respectively. Claims 7 and 9 have been amended according to the examiner's suggestions.

Rejections under 35 USC § 112

Claims 20, 22, and 26 stand rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 1 from which claims 20, 22, and 26 depend has been amended to overcome the examiner's rejection.

Rejections under 35 USC §103

Claims 1-3, 5-8, 10, 17-19, 21, and 23-28 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Lambrecht *et al* (U.S. 5,951,664) in view of Hansen *et al* (U.S. 5,640,490). Claims 4, 9, 12-16, 29-30 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Lambrecht in view of Hansen and further in view of well known prior art (MPEP 2144.03). Claim 11 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Lambrecht in view of Hansen, and further in view of Chang *et al* (U.S. 6,330,247) and Oh *et al* (U.S. 6,275,806).